In the Specification

Please replace the paragraph beginning at page 3, line 21, with the following rewritten paragraph:

In one aspect, the present invention provides a dynamic ~~merging~~ mode processor (DP) capable of dynamically supporting two independent modes of operation and a third unique combined mode of operation in a highly parallel processor comprising an array of processing elements. The third combined mode of operation can be used on highly parallel processors with a very long instruction word (VLIW) architecture given this invention. Dynamically changing modes of operation is defined as modes that can be changed cycle by cycle under programmer control. A combined mode of operation means that in any cycle the two independent modes of operation can be in effect governed by the indirect VLIW (iVLIW) architecture. In a first mode of operation, the DP acts as one of the processing elements in the array and participates in the execution of single-instruction-multiple-data (SIMD) instructions. In a second mode of operation, the DP acts as the controlling element for the array and executes single-instruction-single-data (SISD) instructions. In the third mode of operation, the DP acts simultaneously as the controlling element for the array and as one of the processing elements in the array. This is accomplished when the DP executes an iVLIW instruction containing a combination of SP SISD and PE SIMD type of instructions. To support these three modes of operation, in one presently preferred embodiment of the present invention, an array 200 shown in Fig. 2 includes DP 210 and PEs 220, 230 and 240. DP 210 has a plurality of execution units or functional units 211 which include an instruction sequencer 214. DP 210 also includes two general-purpose register files labeled PE register file 212 and SP register file 213, respectively. The execution units are "shared" in that they can execute instructions while the processor is in either of the first two

modes of operation separately or combined in the third mode of operation. The register files are generally "not shared" in the two separate modes of operation. However, both register files are available for data communications via the array's interconnection network in either mode of operation. By allowing the use of the array's interconnection network as a direct communication path between any PE register file and the SP register file, this structure eliminates the need for a dedicated PE-to-SP data bus. With the ManArray Interconnection Network, the SP is able to broadcast data to the PEs and Receive data from individual PEs in the network. The third combined mode of operation can be obtained by intermixing SP and PE instructions in a VLIW. In this manner, the execution units can be shared between SIMD PE operations and SP SISD operations simultaneously on a cycle by cycle basis all under programmers control with no hazards of operation. This sharing of execution units represents a significant savings in implementation costs. Due to application needs it is possible to have an SP to PE Load Broadcast bus but still not require a PE to SP bus path. This is to improve concurrency of data distribution operation to the array of PEs and thereby improve performance.

Please replace the paragraph beginning at page 4, line 29, with the following rewritten paragraph:

If the mode-of-operation bit is set to a logic "1", a PE mode of operation is indicated. If the mode-of-operation bit is set to a logic "0", an SP mode of operation is indicated. If the PE mode of operation is indicated, every PE in the array, and the DP, acting as another processing element of the array, executes the instruction. If the SP mode of operation is indicated, only the DP, acting as the controlling element of the array, executes the instruction. In a VLIW or iVLIW processor containing multiple instructions of format 300 shown Fig. 3, the SP and PE

modes of operation can be mixed producing unlimited programming flexibility within the capability of the iVLIW or the VLIW architecture ~~VLIWarchitecture~~.

Please replace the paragraph beginning at page 5, line 8, with the following rewritten paragraph:

In a second embodiment of the present invention shown in Fig. 5, an array 500 includes a DP 510 and PEs 520, 530 and 540. The DP 510 includes a plurality of execution units and a single general-purpose register file. The execution units are "shared" in that they can execute instructions while the processor is in either mode of operation. The register file is divided into two banks, a PE bank and [[a]] an SP bank, where the two banks are generally "not shared" in the two separate modes of operation. However, both banks are available for data communications in either mode of operation via the array's interconnection network, enabling the exchange of data between PEs or a PE and the SP.

In the Claims

Claims 1-15 (canceled)

16. (currently amended) An apparatus for concurrently executing controller single instruction single data (SISD) ~~SISD~~ instructions and single instruction multiple data (SIMD) ~~SIMD~~ processing element instructions comprising:

a combined controller and processing element;

a storage device storing a very long instruction word (VLIW) comprising at least ~~two~~ first and second simplex instructions each ~~containing~~ comprising a mode of operation bit, said mode of operation bit in the first simplex instruction specifying a controller SISD operation to be performed by the controller, and the mode of operation bit in the second simplex instruction

specifying a processing element SIMD operation to be performed by the processing element[[;]] ~~and~~

~~very long instruction word (VLIW) containing said at least two simplex instructions.~~

17. (original) The apparatus of claim 16 further comprising a very long instruction word (VLIW) decode and control logic block.

18. (currently amended) The apparatus of claim 17 further comprising a ~~sequence~~ control processor register file and a processing element register file connected to receive write enable control signals from the VLIW decode and control logic block.

19. (original) The apparatus of claim 18 further comprising at least two multiplexers to control the source data path from said register files to inputs of functional units of the combined controller and processing element.

20. (currently amended) The apparatus of claim 16 wherein the combined controller and processing element is connected by an interconnection bus to a plurality of processing elements in ~~a manifold~~ array processing architecture.

21. (new) A processing apparatus comprising:

a merged processor including a control processor and a processing element; and

a memory device communicatively connected to the merged processor for storing a very long instruction word (VLIW), the VLIW comprising a first simplex instruction and a second simplex instruction, each simplex instruction containing a mode of operation bit, the mode of operation bit in the first simplex instruction specifying a controller single instruction single data (SISD) operation to be executed by the controller, and the mode of operation bit in the second simplex instruction specifying a processing element single instruction multiple data (SIMD) operation to be executed by the processing element.

22. (new) The processing apparatus of claim 21 further comprising a VLIW decode and logic control block.

23. (new) The processing apparatus of claim 22 further comprising a control processor register file and a processing element register file, both register files connected to receive control signals from the VLIW decode and control logic block.

24. (new) The processing apparatus of claim 23 wherein the mode of operation bit is used to select the control processor register file or the processing element register file.

25. (new) The processing apparatus of claim 22 further comprising a register file having a processing element bank and a control processor bank.

26. (new) The processing apparatus of claim 25 wherein the mode of operation bit is used to select the control processor register bank or the processing element register bank.

27. (new) The processing apparatus of claim 22 wherein the merged processor is operable to execute the VLIW.

28. (new) The processing apparatus of claim 27 wherein the control processor is operable to execute the control processor instruction in parallel with the processing element executing the processing element instruction.

29. (new) The processing apparatus of claim 21 further comprising a plurality of processing elements and the control processor is operable to control the operation of all processing elements.

30. (new) The apparatus of claim 29 wherein the merged processor and the plurality of processing elements each further comprise at least one register file and an interconnection bus is utilized as a direct communication path between any processing element register file and any register file in the merged processor.

31. (new) A processing apparatus comprising:

a merged processor including a control processor and a processing element, the merged processor operable to execute a very long instruction word (VLIW), the VLIW comprising a first simplex instruction and a second simplex instruction, each simplex instruction containing a mode of operation bit, the mode of operation bit in the first simplex instruction specifying a controller single instruction single data (SISD) operation to be executed by the controller, and the mode of operation bit in the second simplex instruction specifying a processing element single instruction multiple data (SIMD) operation to be executed by the processing element.

32. (new) The processing apparatus of claim 31 further comprising a VLIW decode and logic control block.

33. (new) The processing apparatus of claim 32 further comprising a control processor register file and a processing element register file, both register files connected to receive control signals from the VLIW decode and control logic block.

34. (new) The processing apparatus of claim 33 wherein the mode of operation bit is used to select the control processor register file or the processing element register file.

35. (new) The processing apparatus of claim 32 further comprising a register file having a processing element bank and a control processor bank.

36. (new) The processing apparatus of claim 35 wherein the mode of operation bit is used to select the control processor register bank or the processing element register bank.

37. (new) The processing apparatus of claim 32 wherein the merged processor is operable to execute the VLIW.

38. (new) The processing apparatus of claim 37 wherein the control processor is operable to execute the control processor instruction in parallel with the processing element executing the processing element instruction.

39. (new) The processing apparatus of claim 31 further comprising a plurality of processing elements and the control processor is operable to control the operation of all processing elements.

40. (new) The apparatus of claim 39 wherein the merged processor and the plurality of processing elements each further comprise at least one register file and an interconnection bus is utilized as a direct communication path between any processing element register file and any register file in the merged processor.